AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A semiconductor device comprising:

a first semiconductor region of a first conductivity type, defined by an upper end surface, a lower end surface opposing to the upper end surface, and first and second side boundary surfaces connecting the upper and lower end surfaces when viewed in section;

a second semiconductor region of the first conductivity type having top and bottom surfaces, disposed under the first semiconductor region, a portion of the top surface ~~and~~ being in contact with the lower end surface of said first semiconductor region so as to share a common boundary surface by the first and second semiconductor regions, wherein a first concavity is cut into the bottom surface of the second semiconductor region;

a third semiconductor region of a second conductivity type disposed on the first semiconductor region and being in contact with the upper end surface of said first semiconductor region; ~~and~~

a fourth semiconductor region having first and second inner surfaces in contact with the first and second side boundary surfaces respectively when viewed in section and an impurity concentration lower than said first semiconductor region, configured such that the fourth semiconductor region is disposed between the second and third semiconductor regions; and

a first main electrode layer being in contact with the bottom surface of the second semiconductor region, a part of the first main electrode layer being buried in the first concavity.

2. (Original) The semiconductor device of Claim 1, wherein said fourth semiconductor region has the first conductivity type.

3. (Previously presented) The semiconductor device of Claim 1, wherein outer surface of said fourth semiconductor region serves as a chip outer-surface of the semiconductor device and the chip outer-surface is substantially orthogonal with the lower end surface of said first semiconductor region.

4. (Original) The semiconductor device of Claim 1, wherein said fourth semiconductor region is made of a wafer cut from bulk crystal.

5.-6. (Cancelled).

7. (Currently amended) ~~The semiconductor device of Claim 1,~~ A semiconductor device comprising:

a first semiconductor region of a first conductivity type, defined by an upper end surface, a lower end surface opposing to the upper end surface, and first and second side boundary surfaces connecting the upper and lower end surfaces when viewed in section;

a second semiconductor region of the first conductivity type having top and bottom surfaces, disposed under the first semiconductor region, a portion of the top surface being in contact with the lower end surface of said first semiconductor region so as to share a common boundary surface by the first and second semiconductor regions;

a third semiconductor region of a second conductivity type disposed on the first semiconductor region and being in contact with the upper end surface of said first semiconductor region;

a fourth semiconductor region having first and second inner surfaces in contact with the first and second side boundary surfaces respectively when viewed in section and an impurity concentration lower than said first semiconductor region, configured such that the fourth semiconductor region is disposed between the second and third semiconductor regions; and

a first main electrode layer being in contact with the bottom surface of the second semiconductor region,

wherein the second semiconductor region has a via hole and ~~further comprising a first main electrode layer,~~ a part of the first main electrode layer ~~being~~ is buried in ~~a~~ the via hole penetrating through said second semiconductor region, configured such that the buried part of the first main electrode layer contacts with said first semiconductor region.

8. (Previously presented) The semiconductor device of Claim 1, further comprising a second main electrode layer formed on a top surface of said third semiconductor region.

9. (Previously presented) The semiconductor device of Claim 8, wherein said second main electrode layer is contacted with said third semiconductor region, through a second concavity formed at the top surface of said third semiconductor region.

10.-13. (Cancelled).

14. (New) A semiconductor device comprising:

a first semiconductor region of a first conductivity type, defined by an upper end surface, a lower end surface opposing to the upper end surface, and first and second side boundary surfaces connecting the upper and lower end surfaces when viewed in section;

a second semiconductor region of the first conductivity type disposed under the first semiconductor region and being in contact with the lower end surface of the first semiconductor region so as to share a common boundary surface by the first and second semiconductor regions;

a third semiconductor region of a second conductivity type, having top and bottom surfaces, disposed on the first semiconductor region, the bottom surface being in contact with the upper end surface of the first semiconductor region, wherein a concavity is cut into the top surface of the third semiconductor region;

a fourth semiconductor region having first and second inner surfaces in contact with the first and second side boundary surfaces respectively when viewed in section and an impurity concentration lower than the first semiconductor region, configured such that the fourth semiconductor region is disposed between the second and third semiconductor regions; and

an ohmic contact electrode being in contact with the top surface of the third semiconductor region, a part of the ohmic contact electrode being buried in the concavity.

15. (New) A semiconductor device comprising:

a first semiconductor region of a first conductivity type, defined by an upper end surface, a lower end surface opposing to the upper end surface, and first and second side boundary surfaces connecting the upper and lower end surfaces when viewed in section;

a second semiconductor region of the first conductivity type disposed under the first semiconductor region and being in contact with the lower end surface of the first semiconductor region so as to share a common boundary surface by the first and second semiconductor regions;

a third semiconductor region of a second conductivity type disposed on the first semiconductor region and being in contact with the upper end surface of the first semiconductor region so as to implement a first pn junction interface; and

a fourth semiconductor region having first and second inner surfaces being in contact with the first and second side boundary surfaces respectively when viewed in section and an impurity concentration lower than the first semiconductor region, configured such that the fourth semiconductor region is disposed between the second and third semiconductor regions so that an interface between the third and fourth semiconductor regions implements a second pn junction interface surrounding the first junction interface, the first and second pn junction interfaces establishing a single flat pn junction interface,

wherein outer surfaces of the second, third and fourth semiconductor regions establish a common chip outer surface of the semiconductor device and the chip outer surface is substantially orthogonal with the lower end surface of the first semiconductor region, and a termination of the second pn junction interface is exposed at the chip outer surface.

16. (New) The semiconductor device of Claim 15, wherein the fourth semiconductor region is made of a wafer cut from bulk crystal.